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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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PATENT COUNSEL  
3050 BOWERS AVENUE  
PO BOX 450A  
SANTA CLARA  
CA 95052

IM62/0627

EXAMINER

ZERVIGON, R

ART UNIT	PAPER NUMBER
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1763

DATE MAILED:

06/27/00 *9*

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

File Copy

# Office Action Summary

Application No.

09/362,504

Applicant(s)

Kramadhati et al

Examiner

Rudy Z rvigon

Group Art Unit

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☒ Responsive to communication(s) filed on Mar 6, 2000

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claim

☒ Claim(s) 16-36 is/are pending in the applicat

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration

☐ Claim(s) \_\_\_\_\_ is/are allowed.

☒ Claim(s) 16-36 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

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### **DETAILED ACTION**

1. The 35 U.S.C. 112 second paragraph issues cited in the first office action have been remedied in amendment C received April 4, 2000.

### ***Claim Rejections - 35 USC § 102***

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by Jin Onuki et al. Jin Onuki et al have described improvements in integrated circuit step coverage and electromigration resistance of aluminum films when employing switching bias sputtering (abstract, right column, mid second, last paragraphs page 182). The switching bias sputtering described by Jin Onuki et al are embodied as "two-step bias application" (right column, last paragraph page 182). The two-step bias application is further described by Jin Onuki et al according to a method ordered according to "a deep d.c. bias of -200V, and, second, a shallow d.c. bias of 50V for 10s" (section 2.1 - Film Formation). The method of the Jin Onuki et al process is embodied in repetitive cycles as shown in Figure 1(b). Implicit in the cyclic application of the two-step switching bias sputtering method described by Jin Onuki et al and, according to the step waveforms shown in Figure 1(b), is an unbiased time frame, in each cycle, prior to the application of the first "deep d.c. bias of -200V". It is entrusted that the establishment of a gas in a plasma state necessarily requires "flowing a process gas into a substrate

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processing chamber” and “forming a plasma from said process gas” by “coupling energy into said substrate processing chamber”. Attributes which Jin Onuki et al implicitly establish.

*Claim Rejections - 35 USC § 103*

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 17,18,25-28,32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ye et al (U.S. Pat. 5,710,486) in view of Jin Onuki et al, Boys et al (U.S.Pat. 4,500,408), Ramarotafika et al.

Ye et al describe a substrate processing system comprising:

- i. A housing for forming a vacuum chamber (items 52/54, Figure 3, column 3, lines 49-51)
- ii. A vacuum pump for forming evacuating the vacuum chamber (implied)
- iii. A pedestal (item 60, Figure 3, column 3, lines 52-53), located within the housing for forming a vacuum chamber (items 52/54, Figure 3, column 3, lines 49-51), configured to hold a substrate (item 61, Figure 3, column 3, line 52-53)
- iv. A gas distribution system fluidly coupled to the vacuum chamber (column 3, lines 12-16)
- v. A plasma generation system (column 3, lines 62-67) for forming a plasma from a process gas within housing for forming a vacuum chamber (items 52/54, Figure 3, column 3, lines 49-51).

Ye et al additionally teaches the establishment of a gas in a plasma state by “flowing a process

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gas into a substrate processing chamber” and “forming a plasma from said process gas” by coupling and maintaining energy into said substrate processing chamber.

- vi. Selective biasing of the generated plasma towards the processing substrate is provided according to the independently powered capacitive electrode (item 60, Figure 5) that supports the substrate (Figure 5; column 3, lines 49-67)
- vii. A controller (implied according to column 2, lines 56-59) for controlling plasma generation means

Ye et al do not explicitly discuss a controller (implied according to column 2, lines 56-59) for controlling a vacuum pump and a gas distribution system. And so Ye et al would be modified by adding a controller as taught by Jin Onuki et al.

Jin Onuki et al have introduce improvements in integrated circuit step coverage and electromigration resistance of aluminum films when employing switching bias sputtering (abstract, right column, mid second, last paragraphs page 182). The switching bias sputtering described by Jin Onuki et al are embodied as “two-step bias application” (right column, last paragraph page 182). The two-step bias application is further described by Jin Onuki et al according to a method ordered according to “a deep d.c. bias of -200V, and, second, a shallow d.c. bias of 50V for 10s” (section 2.1 - Film Formation).

The method of the Jin Onuki et al process is embodied in repetitive cycles as shown in Figure 1(b).

Implicit in the cyclic application of the two-step switching bias sputtering method described by Jin Onuki et al and, according to the step waveforms shown in Figure 1(b), is an unbiased time frame,

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in each cycle, prior to the application of the first “deep d.c. bias of -200V”. Thus the Jin Onuki et al reference describe a method of deposition wherein there is selective electrode biasing to deposit a first layer without biasing the generated plasma towards the substrate, and subsequent second layer deposition under biased conditions: “a deep d.c. bias of -200V, and, second, a shallow d.c. bias of 50V for 10s” (section 2.1 - Film Formation). As discussed above, implicit in the cyclic application of the two-step switching bias sputtering method described by Jin Onuki et al and, according to the step waveforms shown in Figure 1(b), is an unbiased time frame, in each cycle, prior to the application of the first “deep d.c. bias of -200V”. Successive cycles, as shown in Figure 1(b), provide additional deposited layers. Ye et al and Jin Onuki et al do not explicitly describe programmable memory controller for controlling the process vacuum pump, gas distribution system.

Boys et al does describe a programmable memory controller for controlling the process vacuum pump, gas distribution system, and plasma generation means. Boys et al further describe a magnetron sputter coating apparatus controlled in response to measurements of plasma parameters to control deposition parameters (abstract). Specifically, Boys et al describe a CPU *computer 57* which includes a conventional memory for storing a program and predetermined data for controlling the operation of sources 25 and 37, as well as orifice 32. The programmed values for the voltage and current of source 37 and the *pressure* in volume 13 are stored in the memory of CPU 57. Additionally, vacuum pump control is discussed according to adding another “variable pumping orifice” (column 8, lines 8-13; column 7, lines 38-40).

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Ramarotafika et al describe the influence of d.c. bias (including unbiased states) of WTi films (section 3).

With the Ye et al apparatus as a footing, a person of ordinary skill in the art at the time the invention was made would consider the control systems as described by Boys et al to be an obvious improvement to the Ye et al apparatus consistent with a deposition method as promoted by Jin Onuki et al and Ramarotafika et al. Motivation for combining the above references follows from the desire to control plasma process attributes as discussed by the Boys et al (column 3, lines 25-67) with a deposition method of Jin Onuki et al supporting sufficient motivation (abstract, right column, mid second, last paragraphs page 182).

6. Claims 19-24,29-31,35,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ye et al (U.S. Pat. 5,710,486) in view of Jin Onuki et al, Boys et al (U.S.Pat. 4,500,408), Ramarotafika et al, as applied to claims 17,18,25-28,32-34 above, and further in view of Matsuura (U.S.Pat. 5,319,247). Jin Onuki et al describes switching bias sputtering power application **embodied as "two-step bias application"** (right column, last paragraph page 182). Matsuura describes a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1). Operating conditions of pressure:  $1\text{mTorr} \leq 100\text{mT} \leq 10\text{Torr}$

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(column 6, line 33) and temperature:  $100^{\circ}\text{C} \leq 350^{\circ}\text{C} \leq 450^{\circ}\text{C} \leq 500^{\circ}\text{C}$  (column 6, line 38) are specifically met by Matsuura.

With the Ye et al apparatus as a footing, a person of ordinary skill in the art at the time the invention was made would consider application of the Matsuura method of forming silicon and oxygen combined thin films for “superior crack resistance and insulation” (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1). Motivation for combining the above references follows from the Matsuura identified improved substrate rigidity, or reducing mechanical stress, and electrical isolation as for “superior crack resistance and insulation” (silicate, column 6, lines 4-11).

### *Response to Arguments*

7. With regards to applicant’s argument that “Onuki et al does not teach or suggest maintaining a plasma to deposit a first layer of a film on a substrate without biasing the plasma toward the substrate....”, the switching bias sputtering described by Jin Onuki et al are **embodied as “two-step bias application”** (right column, last paragraph page 182). The two-step bias application is further described by Jin Onuki et al according to a method ordered according to **“a deep d.c. bias of -200V, and, second, a shallow d.c. bias of 50V for 10s”** (section 2.1 - Film Formation). The method of the Jin Onuki et al process is embodied in repetitive cycles as shown in Figure 1(b). **Implicit in the cyclic application of the two-step switching bias sputtering method described by Jin Onuki et al and, according to the step waveforms shown in Figure 1(b), is an unbiased time frame, in each**



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cycle, prior to the application of the first "deep d.c. bias of -200V". It is entrusted that the establishment of a gas in a plasma state necessarily requires "flowing a process gas into a substrate processing chamber" and "forming a plasma from said process gas". Attributes which Jin Onuki et al implicitly establish.

8. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

9. In response to applicant's argument that the cited references are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the cited references in the field of applicant's endeavor or, specifically, thin film applications mediated through plasma enhanced CVD.

10. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally

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available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, obviousness is, in the Examiner's opinion, established both in this action and the first, by combining or modifying the teachings of the prior art to produce the claimed invention where there teaching, suggestion, and motivation to do so was found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

11. With respect to the applicant's argument's regarding "...the references do not teach or suggest an insulating layer formed between the metal layer and the semiconductor substrate .....", it is precisely taught by Onuki et al that, according to section 2.1: "The 0.5  $\mu\text{m}$  thick Al-0.5wt.%Cu-1wt.%Si films were deposited onto Si wafers with a 0.5 $\mu\text{m}$  thermally grown SiO<sub>2</sub> layer by conventional...". Thus, Onuki et al deposit an insulating layer of silica atop a Si substrate with a overlying layer containing a metallic components. This is precisely depicted in figure 4 and associated discussions.


### *Conclusion*

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Rudy Zervigon whose telephone number is (703) 305-1351. The examiner can normally be reached on a Monday through Thursday schedule from 8am through 7pm. The official after final fax phone number for the 1763 art unit is (703) 305-3599. Any Inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Chemical and Materials Engineering art unit receptionist at (703) 308-0661. If the examiner can not be reached then please contact the examiner's supervisor, Gregory L. Mills, at (703) 308-1633.

  
GREGORY MILLS  
PRIMARY EXAMINER  
SPE 1763